FPGA Controller Based Experimental Analysis of A Cascaded Hybrid Bridge Seven Level Inverter

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***Abstract*— In today's era, reliable and good quality power is an essential requirement in industry, which can be supplied by inverters at medium and high power. Most of the appliances in the industry require high power or medium power for their operation. Power electronics devices such as inverters work on medium voltage and high power and are suitable for industrial applications. Multilevel inverters are more superior to conventional inverters because of lower harmonics and switching losses, but as the number of levels increases, complexity also increases. Therefore, maintaining the harmonics at lower level and lesser complexity of multilevel inverters is a challenge for researchers. In this research paper, a novel approach for implementation of seven level cascaded hybrid bridge configuration of multilevel inverter using direct current source and photovoltaic panels is being used. The basic working principle of seven level cascaded hybrid bridge inverter, pulse width modulation techniques and total harmonic distortion are explained through simulations in Matlab and Xilinx 14.3 software and the same is experimentally validated through FPGA controller based Spartan 6. The designed seven level inverter results in lower total harmonic distortion with lesser complexity as the number of switching devices is thirty six only. The designed seven level inverter can be further used in reactive power compensation devices such as static synchronous compensator for better control of active and reactive power.**

Keywords*—Multilevel Inverter; Cascaded Hybrid Bridge; Photovoltaic; Direct Current; Alternating Current; Total Harmonic Distortion

I. INTRODUCTION

With the development of technology, power electronics have became an integral part of our daily life such as transportation, residential, industrial, telecommunication and aerospace applications. Nowadays, many industrial applications require high power. In such industrial applications, power electronics converters such as multilevel inverters (MLIs) are highly recommended because of its prominent features such as reduced harmonics, minimum switching losses, electromagnetic compatibility and good power quality etc. at medium voltage and high power [1-2]. Electric power is used in almost every aspect and everywhere in modern human society. Electric power is the major form of energy source used in today's world. The objective of MLIs is to provide the improved power quality, effective control and efficient utilization of electric power. It is estimated that in developed countries now 60% of the electric energy goes through some kind of power inverters before it is finally used. Nowadays, MLIs have been making major contributions to: 1) better control of electric equipment, 2) reduction of energy consumption leads to less pollution, 3) improve the efficiency by making reliable operation of semiconductor devices, 4) better sinusoidal output waveform with minimum harmonics and 4) enhance the voltage profile.

MLIs have been introduced since 1975 as an alternative in high power applications [3-5]. Compared with conventional inverters, MLIs deal with more than two voltage levels. Voltage levels are combined in MLIs and the generated waveform results in better output waveform, minimum total harmonic distortion (THD), minimum switching losses and lesser electromagnetic interferences. However, as the number of levels increases in MLIs, complexity also increases because of increased switching devices. Therefore, to maintain the balance between the complexity and harmonics in MLIs is also a challenge. MLIs can be used in numerous applications such as high voltage direct current transmission, flexible alternating current transmission, static var compensation and harmonic suppression, energy storage systems and supplemental energy sources for e.g. wind, photovoltaic and fuel cells etc.

Neutral point clamped (NPC), flying capacitor (FC) and cascaded hybrid bridge (CHB) are the three different available topologies of MLIs [6]. The difference in all these topologies lies in the mechanism of switching and source of input to the MLIs. Compared with NPC and FC topology, CHB topology requires the minimum number of components and avoids the requirement of clamping diodes and capacitors as in NPC and FC topology respectively. The technical and economical factor suggests the use of CHB topology for industrial applications [7-8]. CHB topology has the potential for utility interface applications because of its capabilities for applying modulation and soft switching techniques [9-10].

The interfacing of MLIs having more number of levels and renewable energy sources is a major concern in today's world for grid and micro grids applications [11-13]. Utilization of renewable energy sources such as wind and solar energy is more advantageous in both environmentally and economically. In India, Ministry of New and Renewable Energy (MNRE) has proposed to speed up the renewable sources utilization to about 227 GW by 2022, with 90% volume is accounted by solar and wind energy [14]. More and more renewable energy sources deployment leads to benefits such as energy security, economic benefits as well as better environmental conditions [15-16]. Tremendous research work is going on photovoltaic (PV) generation systems for effective utilization of solar energy.

In this research paper, multilevel inverter having seven levels with CHB topology is simulated and the same is validated through experimental study. Seven level CHB inverter is designed using DC source as input signal and then using PV cells rather than DC source as input signal. Seven level CHB inverter with PV cells takes more time to simulate than with DC source. The generated MATLAB code of seven level CHB inverter with DC source is further converted into Xilinx code. Through Xilinx, coding is downloaded onto a FPGA Spartan 6 XC6SLX9 board and finally to the hardware of seven level CHB inverter. Maintaining the balance between the complexity and harmonics, the implemented multilevel inverter results in lesser complexity (as the number of levels is seven), lower harmonics as well as lower losses. The designed inverter can be used for generating staircase sinusoidal waveform from the DC input with lower THD.

II. OPTIMIZATION TECHNIQUES FOR MULTILEVEL INVERTERS

Optimization techniques are required for proper selection of firing angles in MLIs [27-29]. For seven level CHB inverter, three firing angles are there, therefore good choice of these three angles is must to keep the harmonics at lower level. This is done with the aid of optimization techniques. Numerous optimization techniques are available in the literature such as Newton Raphson numerical technique, theory of resultant and symmetrical polynomials, generalized pattern search, genetic algorithm, simulated annealing and particle swarm optimization (PSO) etc. [30-32]. In this research work, PSO technique is used for calculation of three optimized firing angles of seven level CHB inverter. Following steps are involved in the proposed PSO algorithm of seven level CHB inverter:

Step I: Formulation of objective function

Mathematically, 5th and 7th harmonics of CHB seven level inverter can be shown as below:

$$V_{5th} = \cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3$$
$$V_{7th} = \cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3 \quad (1)$$

To minimize these harmonics, defined objective function is:

$$Y = \{abs(V_5) + abs(V_7)\} \quad (2)$$

Step II: Initialization

First step involves the initialization of the parameters such as velocity, position, local best position and the global best position of the particles and swarm respectively, by taking into account the constraints of the three firing angles.

Step III: Updating the personal best position

According to the best position of the individual particles, update the personal best position.

Step IV: Updating the global best position

According to the best position of the swarm, update the global best position.

Step V: Criterion for exit

After achieving a good fitness value, optimization procedure needs to be stopped. This ultimately results in the three optimized firing angles for cascaded seven level inverter.

Generally, proper selection of switching angles results in elimination of low frequency harmonics and by using additional filter circuits, high frequency harmonics are eliminated. The optimized three firing angles of seven level CHB inverter are calculated using PSO algorithm at modulation index 0.75 i.e. 34.8935, 54.4622 and 68.5500 degree. The phase voltage and line to line voltage THD is calculated using the formula:

$$THD = \frac{\sqrt{\sum_{N=2}^{200}\left[\frac{1}{N}\left(\cos\left(N\alpha_1\right)+\cos\left(N\alpha_2\right)+.....+\cos\left(N\alpha_s\right)\right)\right]^2}}{\left[\cos\left(\alpha_1\right)+\cos\left(\alpha_2\right)+.....+\cos(\alpha_s)\right]} \quad (3)$$

III. SIMULATIONS AND EXPERIMENTAL RESULTS

MLIs are required for producing sinusoidal output voltage waveform with lesser harmonics. In this research work, two cases are taken. First case, involves the simulation of seven level CHB inverter with DC source as input and the second case represents the simulation of same inverter with PV panels as input. Table 1 represents the switching pattern of the designed seven level CHB inverter.

Table 1 Defined Switching States for Seven Level CHB MLI

Output Voltage Vo	Switching States S11	S31	S12	S32	VH 1	VH2
3E	1	0	1	0	E	2E
E	1	1	1	0	0	2E
	0	0	1	0	0	2E
E	1	0	1	1	E	0
	1	0	0	0	E	0
	0	1	1	0	-E	2E
0	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
-E	1	0	0	1	E	-2E
	0	1	1	1	-E	0
	0	1	0	0	-E	0
-2E	1	1	0	1	0	-2E

H-bridge block used is for seven level CHB inverter, having three h-bridges per phase, say H_1, H_2 and H_3. Each H bridge consists of four IGBTs, making total 12 switches per phase. Therefore, total 36 IGBTs switches are there in the seven level CHB inverter. Three h-bridges of each phase are connected with DC source as shown in fig 8, while in another case these h-bridges are connected to PV panel rather than DC source. In both cases, the designed seven level CHB inverter is same, only difference is in the input source i.e. first one is using DC source and second is using PV panel. Both cases, staircase seven level output is obtained but with PV panels, THD is low as compare to TDH with DC source. Simulation time is more in the second case (taking 20 minutes to execute) because of the complex block and subsystem of PV cells while in first case direct DC source is taken so it takes only five minutes to execute. Next step is to provide firing to the IGBTs switches of h-bridge. Firing should be provided in such a way so that first h-bridge (four IGBTs switches) is fired first, then after phase shift of 120°, next h-bridge is fired and after 240°, last h-bridge is fired so that for complete cycle, stepped sinusoidal waveform is obtained. This is done using PWM control strategy. Selection of control strategy is the foremost step in designing of inverter. Using PSO, optimal angles i.e. 34.8935, 54.4622 and 68.5500 degree at modulation index 0.75 are obtained as shown in table 2. IGBTs switches are then fired and ultimately THD is obtained, which is very low. Therefore, the adopted technique in this research work is useful for obtaining staircase sinusoidal output in the multilevel inverter (seven level in this case, can be applied to the higher levels of inverters). Also, the designed inverter can be further used in another applications such as reactive power compensation (in static synchronous compensators) etc., which is very important and useful for large scale industries.

Table 2 Calculated Switching Angles of Cascaded Seven Level Inverter using PSO

Modulation Index M	α1(degree)	α2(degree)	α3(degree)
1.00	11.6817	31.1783	58.5774
0.90	17.5104	43.0523	64.1395
0.85	22.7654	49.3798	64.5562
0.80	29.2355	54.4383	64.4844
0.75	34.8935	54.4622	68.5500
0.70	38.3413	53.9297	73.9648
0.65	39.3876	55.5215	78.8979
0.60	39.4298	58.5839	83.1042

Simulation results for the designed seven level CHB inverter using optimized PWM and PSO techniques are presented in fig. 1-5. Fig. 1 represents the staircase output voltage levels obtained from the designed seven level CHB inverter after simulation in MATLAB and Xilinx software. Fig. 2-4 shows the three firing pulses required for the firing of H-bridges. In the proposed seven level CHB inverter, at modulation index 0.75, optimized firing angles are obtained, which further leads to better output waveform in comparison to traditional results. In addition, THD is low with lesser simulation time for DC sources as represented in fig. 5. Therefore, from the simulation results, it can be concluded that with the aid of proposed seven level CHB inverter, staircase output waveform with minimum distortions are obtained.

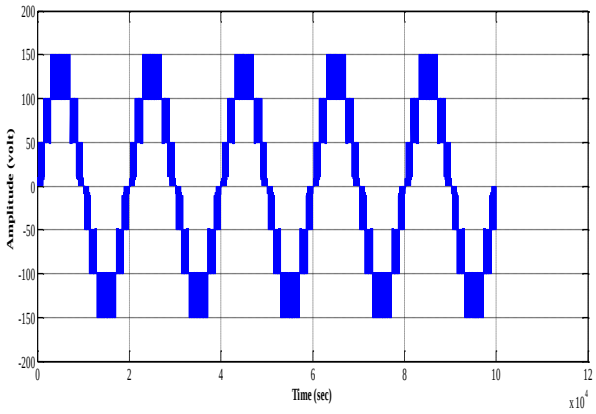

Fig. 1 Simulated Voltage Levels in the CHB Inverter

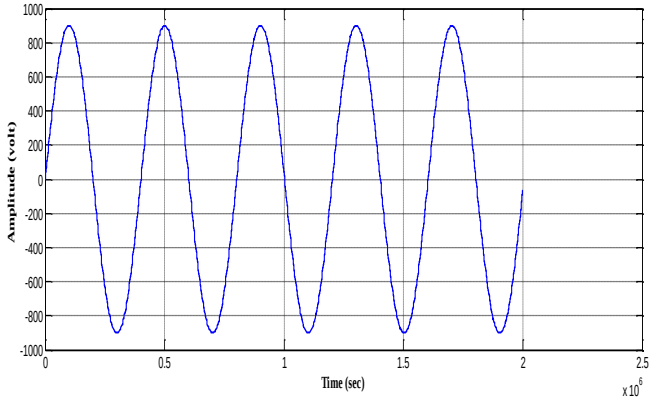

Fig. 2 First Firing Pulse to CHB Inverter

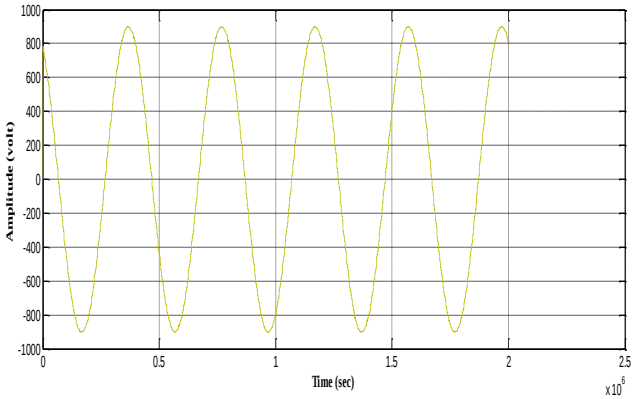

Fig. 3 Second Firing Pulse to CHB Inverter

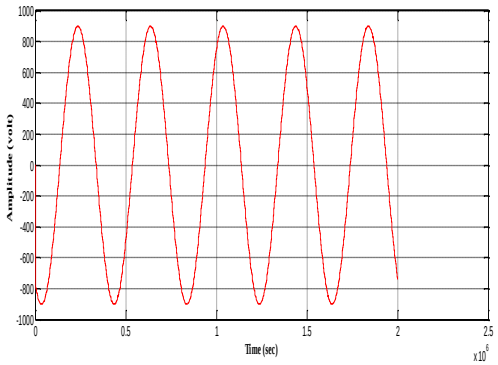

Fig. 4 Third Firing Pulse to CHB Inverter

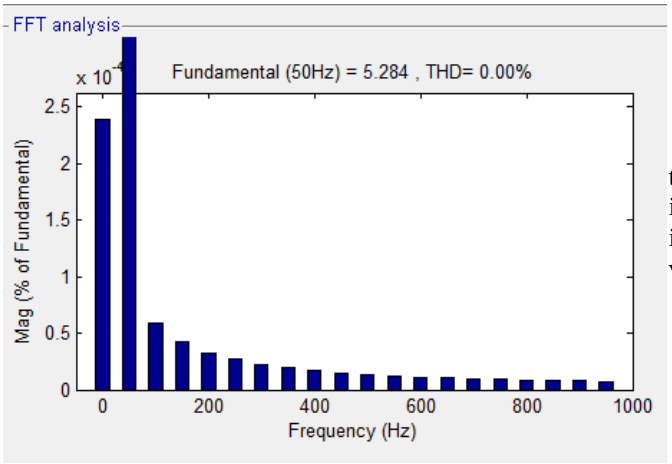

Fig. 5 FFT Analysis of designed 7 Level CHB Inverter

Experimental results with a seven level CHB inverter (as shown in fig. 6) were performed to validate the simulations. The traditional PWM and the proposed PWM technique for designed seven level CHB inverter were implemented using a FPGA controller based Spartan 6. In the FPGA controller based Spartan 6 board, the designed seven level CHB inverter coding is burnt, which provides the signals to CHB seven level inverter and finally the waveforms are observed on power analyzer.

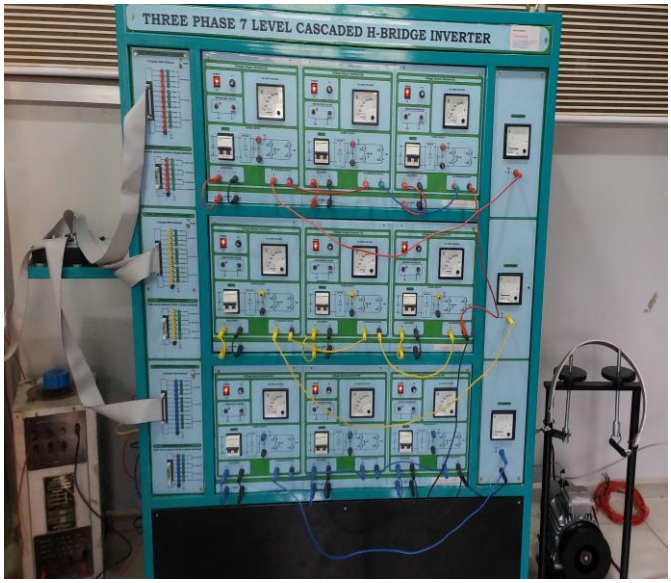

Fig. 6 Seven Level CHB Inverter connected with Spartan 6 and Induction Motor

Through the designed coding of seven level CHB inverter, the speed of induction motor is also controlled as represented in table 3, where the input voltage through transform is varied in steps, corresponding readings of DC link voltage, line voltage and speed of induction motor are shown.

Table 3 Experimental Readings of Voltages of CHB 7 Level Inverter

Input Voltage through transformer (Vin in volt)	DC Link Voltage (Vdc in volt)	Line Voltage (Vl in volt)	Induction Motor Speed (rpm)
20	5.51	8.92	5.91
30	11.62	20.82	530
40	13.96	30.05	1294
50	16.91	37.37	1304
60	20.93	46.54	1402
70	24.14	55.78	1392
80	27.61	67.34	1390
90	32.92	79.28	1420

IV. Conclusion

Among the existing MLIs topologies, CHB topology is the most promising alternative for the PV applications. Same number of output voltage levels can be achieved using CHB topology with fewer switches as compared to other topologies. The control complexity associated with CHB configuration is directly proportional to the number of H-bridges used. In this research work, three H-bridges per phase are used, therefore, the complexity associated with the seven level CHB inverter is less. In terms of switching losses and THD, seven level CHB inverter provides satisfactory results. Also the use of PV cells rather the DC sources are more economical and environmental friendly. Seven level CHB inverter with DC source and PV panel is implemented in MATLAB and Xilinx software and finally the coding is experimentally validated. With the aid of proposed research work, sinusoidal output waveforms with fewer harmonics are obtained for a seven level CHB inverter. Also, the speed of induction motor is successfully controlled using the designed seven level CHB inverter. Authors will also like to investigate the designed inverter for reactive power compensation devices such as STATCOM.

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